Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) An integrated circuit comprising:

a memory array having at least a first plane[[,]] and a second plane, ~~a third plane, and a fourth plane,~~ wherein a first partition of the memory array comprises one of the planes and a second partition of the memory array comprises the remaining planes, wherein a write operation is to be performed on the first partition and a read operation is to be concurrently performed on the second partition; and

a status register coupled to the memory array, wherein the status register is to provide ~~provides~~ status information ~~of the first plane, the second plane, the third plane, and the fourth plane~~ for at least the first and second planes, the status register being responsive to a memory address associated with one of the first and second partitions to indicate a status of the addressed partition.

2. (Canceled)

3. (Previously Presented) The integrated circuit of claim 1, further comprising:

a microcontroller coupled to the status register, wherein the microcontroller supplies control signals to the status register.

4. (Currently Amended) The integrated circuit of claim 1, wherein the at least first ~~plane, the~~ and second ~~plane, the third plane, and the fourth plane~~ planes comprise substantially equal memory storage capacities.

5. (Currently Amended) The integrated circuit of claim 3, further comprising:

an user interface coupled to the status register, wherein the user interface is to communicate[[s]] status register information to be used to decide subsequent operations.

6. (Currently Amended) A method of reading while writing to a memory array, comprising:

dividing the memory array into n planes, wherein n is an integer greater than ~~two~~ one;

defining a write partition, wherein the write partition is a single plane of the memory array;

defining a read partition, wherein the read partition is made up of all of the remaining n-1 planes of the memory array; and

providing the status of the read partition and the write partition of the memory array with a single status register, wherein providing the status includes providing the status of the read partition responsive to receiving an address associated with the read partition and providing the status of the write partition responsive to receiving an address associated with the write partition.

7. (Currently Amended) The method of claim 6, wherein the memory array consists of multiple ~~4M-b~~ memory planes having substantially equal storage capacity.

8. (Currently Amended) The method of claim 7, wherein the multiple ~~4M-b~~ memory planes consist of nonvolatile memory cells.

9. (Original) The method of claim 8, wherein the nonvolatile memory cell is a flash memory cell.

10. (Original) The method of claim 7, wherein the write partition has a dynamic memory address, wherein the memory address changes any time a program or erase operation begins or resumes in a new memory plane.

11. (Original) The method of claim 7, wherein if no program or erase operation is performed, the read partition and the write partition are allocated to the same memory location.

12.-17. (Canceled)

18. (Previously Presented) An apparatus comprising:

means for partitioning a memory array into a fixed first partition and a variable second partition to enable multiple operations to be performed on the memory array at the same time; and

means for monitoring the operations performed on the memory array.

19. (Original) The apparatus of claim 18 further comprising a means for communicating the status of the operations performed on the memory array to a user.